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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,509	07/16/2004	Gaurav Kumar VARSHNEY	TI-38654	4508

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,509	VARSHNEY ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 45-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 45-64* is/are rejected.

7)☒ Claim(s) *6-18 and 50-62* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/710,509, and Amendment filed on 10/26/06. Claims 21-44 and 65-88 have been cancelled. Claims 1-20 and 45-64 remain pending in the application.

Claim Objections

2. Claims 1 and 45 are objected to because following informalities:

Applicant must clarify what is "a **set** of input pins **other** than said **input pin**".

3. Claim 4 is objected to because following informalities:

Applicant must clarify what is "at least **three immunity transition points for** each of said vectors".

Appropriate corrections are required.

Specification

4. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)),

and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Content of Specification

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

5. "**Summary of the invention**" is missed in the specification.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1- 5, 19-20, 45-49 and 63-64 are rejected under 35 U.S.C. 102(e) as being unpatentable by Chandra et al. (US Pub. No.: 20030145296).

7. As to claims 1 and 45 Chandra discloses:

(1) A method of reducing computational resources in characterizing a parameter for a combination of an input pin and an output pin of a cell (There needs to be a sufficient energy in the input noise signal to affect output change. The width of the noise (in this case measured at the 50% point of the noise value) can be a determining factor – [0023]), said cell being contained in a library used in the design of an integrated circuit (The automation of the vector generation is achieved by using the function description of the cell in the synthesis library - [0061]), said method comprises:

determining a worst case vector (The characterization required for the analysis uses the worst case value today ... The input vectors are set to provide the minimum Wn and Wp effective width for the low and high noise calculations, respectively – [0086]), wherein said worst case vector represents a set of input bits, with each of said input bits being applied to a corresponding one of a set of input pins other than said

input pin of said combination (For example, in case of the circuit 800 in FIG. 8 the beta.n/beta.p is maximized by maximizing the effective width of the n tree by setting A2 and A3 to logic 1 value to get a conservative value of VIL In other words, to get VIL, vary the DC voltage on the input A1 from low to high in steps while keeping A2=A3=1 – [0060] ... In a more complex gate 900 as shown in FIG. 9 the p transistors H, B, C1 are sensitized to logic "0" while switching the D input during the DC characterization. The function beta.n/beta.p is maximized for the conservative value of VIL. A converse set of sensitization vectors are used for the side input signals for the VIH characterization such that a conservative value can be obtained. In case of the complex gate 900 in FIG. 9 - [0061]), wherein said worst case vector would cause propagation of most noise from said input pin to said output pin among vectors which would cause a bit value transition on said output pin if the input bit value is changed on said input pin (generating DC noise margin data and AC noise margin data for a data line of said given cell includes: ... inject noise on said data line within a setup time of said given cell, said noise injected with changing height and width until a output line of said given cell shows a change in state – claim 13) ([0060]- [0063]; claim 13); and

computing a plurality of data values for said parameter when said worst case vector is applied to said set of input pins (For each switching input pin the vector set of the side input pins are chosen ... The switching input is then subjected to simulation using triangular waveforms. The width of the triangle is determined by using the signal transition times as specified in the timing library for the cell, the width being measured at 50% of the height. ... Each transition time yields a particular signal width and a family of

curves is generated as shown in FIG. 5. Then using the load values in the timing table a family of noise rejection curves are generated for the gate as shown in FIG. 6 ... The default is to let the tool automatically collect data for-all pins and select the worst- case values for the cell level - [0062]; [0063]) ([0045]; [0062]; [0063]; [0086]; claim 15),

wherein said plurality of data values are used in an analysis of said integrated circuit irrespective of which of said vectors is applied to said set of input pins (A methodology is disclosed, parallel to timing verification, where the cell library is pre-characterized for the noise margins at the input pins so that tools can look at the specific environment of each instance of the library cell and verify that the computed noise on the input nets of the cell(s) are within acceptable limits. Based on such an analysis implementation decisions can be made to avoid signal crosstalk noise violations - ([0045]; [0086]);

(5) A machine readable medium carrying one or more sequences of

instructions for causing a system to reduce computational resources in characterizing a parameter for a combination of an input pin and an output pin of a cell, said cell being contained in a library used in the design of an integrated circuit, wherein execution of said one or more sequences of instructions by one or more processors contained in said system causes said one or more processors to perform the actions of ([0023]; [0061]; claim 22):

determining a worst case vector (The characterization required for the analysis uses the worst case value today ... The input vectors are set to provide the minimum Wn and Wp effective width for the low and high noise calculations, respectively –

[0086]), wherein said worst case vector represents a set of input bits, with each of said input bits being applied to a corresponding one of a set of input pins other than said input pin of said combination (For example, in case of the circuit 800 in FIG. 8 the beta.n/beta.p is maximized by maximizing the effective width of the n tree by setting A2 and A3 to logic 1 value to get a conservative value of VIL In other words, to get VIL, vary the DC voltage on the input A1 from low to high in steps while keeping A2=A3=1 – [0060] ... In a more complex gate 900 as shown in FIG. 9 the p transistors H, B, C1 are sensitized to logic "0" while switching the D input during the DC characterization. The function beta.n/beta.p is maximized for the conservative value of VIL. A converse set of sensitization vectors are used for the side input signals for the VIH characterization such that a conservative value can be obtained. In case of the complex gate 900 in FIG. 9 - [0061]), wherein said worst case vector would cause propagation of most noise from said input pin to said output pin among vectors which would cause a bit value transition on said output pin if the input bit value is changed on said input pin (generating DC noise margin data and AC noise margin data for a data line of said given cell includes: ... inject noise on said data line within a setup time of said given cell, said noise injected with changing height and width until a output line of said given cell shows a change in state – claim 13) ([0060]- [0063]; claim 13); and

computing a plurality of data values for said parameter when said worst case vector is applied to said set of input pins (For each switching input pin the vector set of the side input pins are chosen ... The switching input is then subjected to simulation using triangular waveforms. The width of the triangle is determined by using the signal

transition times as specified in the timing library for the cell, the width being measured at 50% of the height. ... Each transition time yields a particular signal width and a family of curves is generated as shown in FIG. 5. Then using the load values in the timing table a family of noise rejection curves are generated for the gate as shown in FIG. 6 ... The default is to let the tool automatically collect data for-all pins and select the worst- case values for the cell level - [0062]; [0063]) ([0045]; [0062]; [0063]; [0086]; claim 15),

wherein said plurality of data values are used in an analysis of said integrated circuit irrespective of which of said vectors is applied to said set of input pins (A methodology is disclosed, parallel to timing verification, where the cell library is pre-characterized for the noise margins at the input pins so that tools can look at the specific environment of each instance of the library cell and verify that the computed noise on the input nets of the cell(s) are within acceptable limits. Based on such an analysis implementation decisions can be made to avoid signal crosstalk noise violations - ([0045]; [0086]).

8. As to claims 2-5, 19-20, 46-49 and 63-64 Chandra recites:

(2), (3) (46), (47) The method/program, wherein said determining comprises applying a plurality of glitches to said cell for each of said vectors ([0062]; [0063]);

(4), (5) (48), (49) The method/program, wherein said applying and said examining determine at least three immunity transition points for each of said vectors ([0062]; [0086]- [0089]);

(19), (20) (63), (64) The method/program, wherein said cell comprises a sequential element ([0069]- [0081]; claim 13).

Allowable Subject Matter

9. Claims 6-18 and 50-62 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 6-18 would and 50-62 be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 6)

wherein said parameter comprises noise immunity, wherein a failure result is deemed to be obtained for an input glitch of a first height and a first width if the height of an output glitch corresponding to said input glitch exceeds a first threshold voltage, and a success result is deemed to be obtained otherwise, said method further comprises generating a noise immunity curve (NIC) corresponding to only said worst case vector, wherein said NIC contains a plurality of immunity transition points, wherein each of said plurality of immunity transition points indicates a minimum value for one dimension of said input glitch required for said failure result for each of a value of the other dimension.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

THUAN V. DO
PRIMARY PATENT EXAMINER

12/21/06